CLAIMS

What is claimed is:

1. A method for dynamically controlling an output driver stage comprising:

sensing a signal from an output from said output driver stage; and

controlling said output driver stage based on said sensed signal.

2. The method of claim 1 wherein said output driver stage comprises two or more stacked transistors.

3. The method of claim 2 wherein said two or more stacked transistors are configured in a cascode mode.

4. The method of claim 2 wherein said sensed signal and said controlling are separated by less than two gate delays in time.

5. An apparatus comprising:

means for sensing a signal from an output driver stage; and

means for controlling said output driver stage based on said sensed signal.

6. The apparatus of claim 5 wherein said means for sensing is selected from the group consisting of a resistive means, a transmission gate means, a P channel transistor means, a N channel transistor means, and a capacitive means.

7. The apparatus of claim 5 wherein said output driver stage comprises two or more stacked transistors.

8. A machine-readable medium having stored thereon information representing the apparatus of claim 5.

9. A circuit comprising:

a first transistor having a control terminal, an input terminal, and an output terminal, wherein said first transistor control terminal is coupled to a first feedback control block output and said first transistor input terminal is coupled to receive a positive supply voltage;

a second transistor having a control terminal, an input terminal, and an output terminal, wherein said second transistor control terminal is coupled to receive a data signal and said second transistor input terminal is coupled to said first transistor output terminal;

a third transistor having a control terminal, an input terminal, and an output terminal, wherein said third transistor control terminal is coupled to receive said data signal and said third transistor output terminal is coupled to said second transistor output terminal;

a fourth transistor having a control terminal, an input terminal, and an output terminal, wherein said fourth transistor control terminal is coupled to a second feedback control block output, said fourth transistor output terminal is coupled to said third transistor input terminal, and said fourth transistor input terminal is coupled to receive a supply voltage less positive than said positive supply voltage;

a first feedback control block having an input and said first feedback control block output, wherein said first feedback control block input is coupled to said second transistor output terminal; and

a second feedback control block having an input and said second feedback control block output, wherein said second feedback control block input is coupled to said third transistor output terminal.

10. The circuit of claim 9 further comprising:

a fifth transistor having a control terminal, an input terminal, and an output terminal, wherein said fifth transistor control terminal is coupled to receive said data signal, said fifth transistor input terminal is coupled to receive said positive supply voltage, and said fifth transistor output terminal is coupled to said second transistor output terminal.

11. The circuit of claim 9 further comprising:

a sixth transistor having a control terminal, an input terminal, and an output terminal, wherein said sixth transistor control terminal is coupled to receive said data signal, said sixth transistor input terminal is coupled to receive said supply voltage less positive than said positive supply voltage, and said sixth transistor output terminal is coupled to said third transistor output terminal.

12. The circuit of claim 9 further comprising:

a fifth transistor having a control terminal, an input terminal, and an output terminal, wherein said fifth transistor control terminal is coupled to receive said data signal, said fifth

transistor input terminal is coupled to receive said positive supply voltage, and said fifth transistor output terminal is coupled to said second transistor output terminal; and

a sixth transistor having a control terminal, an input terminal, and an output terminal, wherein said sixth transistor control terminal is coupled to receive said data signal, said sixth transistor input terminal is coupled to receive said supply voltage less positive than said positive supply voltage, and said sixth transistor output terminal is coupled to said third transistor output terminal.

13. The circuit of claim 9 wherein said first feedback control block comprises a transmission gate.

14. The circuit of claim 9 wherein said second feedback control block comprises a transmission gate.

15. The circuit of claim 9 wherein said first feedback control block and said second feedback control block each contain a device selected from the group consisting of transmission gate, resistor, capacitor, p channel transistor, and n channel transistor.

16. A machine-readable medium having stored thereon information representing the apparatus of claim 9.

17. A method comprising:

receiving an input signal;

driving at least one transistor in a stacked output transistor array having two or more transistors;

sampling an output of the stacked output transistor array; and

transferring a signal based on said sample of the stacked output transistor array to one or more transistors in said stacked output transistor array.

18. A method comprising:

generating an output signal;

receiving said output signal; and

feeding back a signal based on said received output signal to at least one transistor in a stacked output transistor array having two or more transistors.

19. The method of claim 18 wherein said feeding back passes said output signal through a device selected from the group consisting of a resistor, a capacitor, a n type transistor, and a p type transistor.

20. The method of claim 19 wherein said feeding back further comprises a comparison of said received output signal to a reference voltage.

21. The method of claim 20 wherein said stacked output transistor array substantially generated said output signal.

22. A method comprising:

receiving an input signal;

driving at least one transistor in a first stacked output transistor array having two or more transistors at a first time;

driving at least one transistor in a second stacked output transistor array having two or more transistors at a second time;

sampling an output of said first stacked output transistor array and said second stacked transistor array; and

transferring a signal based on said sample of said first stacked output transistor array and said second stacked output transistor array to one or more transistors in said first stacked output transistor array.

23. The method of claim 22 further comprising transferring a signal based on said sample of said first stacked output transistor array and said second stacked output transistor array to one or more transistors in said second stacked output transistor array.

24. A method comprising:

driving one or more transistors connected in series to produce an output;

feeding back to said one or more transistors a portion of said output.

25. The method of claim 24 wherein said feeding back connects said output to said one or more transistors through a device selected from the group consisting of a NMOS device, a PMOS device, a resistive component, and an inductive component.

26. The method of claim 24 wherein said one or more transistors are directly connected to said output.

27. The method of claim 24 wherein said one or more transistors are directly connected to a supply voltage.

28. An apparatus comprising:

a first transistor having a source, a drain, and a gate wherein said first transistor source is connected to a voltage;

a second transistor having a source, a drain, and a gate wherein said second transistor source is connected to said first transistor drain, said second transistor gate is connected to an input, and said second transistor drain is an output;

a feedback device having an input and an output, said feedback device input connected to said output, and said first transistor gate connected to said feedback device output.

29. The apparatus of claim 28 wherein said feedback device is selected from the group consisting of a transmission gate, a p channel transistor, an n channel transistor, a resistor, and a capacitor.

30. The apparatus of claim 28 wherein said feedback device contains one or more devices selected from the group consisting of a transmission gate, a p channel transistor, an n channel transistor, a resistor, and a capacitor.